Department of Electrical and Computer Engineering
University of California Davis
EEC146A Integrated Circuits Fabrication
Fall Quarter 2015

Instructor:
Dr. Erkin Şeker
Dept. of Electrical and Computer Engr.
Rm. 3177, Kemper Hall
Email: eseker@ucdavis.edu
Office Hours: Tue. 11:00am-12:00pm and Wed. 11:00-12:00pm in 3177 Kemper

Microfabrication Engineer:
Dr. Yusha Bey
Email: jasmall@ucdavis.edu

TAs:
Josh Garrison
Email: jcgarrison@ucdavis.edu

Gurkan Polat
Email: kgpolat@ucdavis.edu

Jackson Thomas
Email: jakthomas@ucdavis.edu

TAs will not hold regular office hours and should be contacted via email to schedule meetings if needed.

Lecture Times:		**Location:**
Tue. and Thu.	9:00am-9:50am	Wellman, Rm. 115

Lab Times:		**Location:**	**TA:**
Monday	9:00-11:50am	Kemper Hall 1224	Josh Garrison
Wednesday	1:10-4:00pm	Kemper Hall 1224	Gurkan Polat
Thursday	1:10-4:00pm	Kemper Hall 1224	Jackson Thomas

Catalog Description:
Integrated Circuits Fabrication: (3 units) Lecture 2 hours; Lab 3 hours.

Basic fabrication processes for Metal Oxide Semiconductor (MOS) integrated circuits. Laboratory assignments covering oxidation, photolithography, impurity diffusion, metallization, wet chemical etching, and characterization work together in producing metal-gate PMOS test chips which will undergo parametric and functional testing.

Prerequisites:
EEC 140A

Textbook:
Required: *Introduction to Microelectronic Fabrication, 2nd Edition* by Richard C. Jaeger. Prentice Hall, McGraw Hill, 2002.

Suggested reading: *Silicon VLSI Technology – Fundamentals, Practice, Modeling* by James D. Plummer, Michael D. Deal, Peter B. Griffin. Prentice Hall, 2000.

Grading:
Homework: 5%
Weekly Labs: 35% (Pre-lab: 15% & Lab report: 20%)
Midterm Exam: 20%
Quiz (15%)
Final Exam: 25%

Homework Sets:
There will be 7-8 homework sets which will typically be assigned a week before they are due. Homework will not be graded in detail but a full or no score will be administered for each question.

Laboratory Assignments:
A pre-lab homework will be assigned approximately a week before each lab. In order to benefit fully from the lab session, it is essential to complete these assignments. More information on the pre-lab and lab report assignments will be given in class and by the TAs.

Quizzes:
Unannounced in class quizzes (~10 minutes long) will be given during class. Students will be required to provide their own blank paper to take the quiz. There will be approximately 10 quizzes during the entire quarter and the lowest grade will be dropped. There will be no make-up quizzes or time extension for late starts.

Final Exam:
Final exam is scheduled for 6:00pm-8:00pm Friday December 8, 2015. Final exam will be comprehensive. Further information will be given in-class prior to each exam.

Make-up Exams:
Make-up exams will not be given unless cases of extreme extenuating circumstances arise.

Regrading:
If you disagree with the grading on homework, quiz, or exams with good reason please attach a note and return it to the instructor. The instructor will review the grading, and reassign points as necessary. Note that upon regrading the score may go up or down.

Attendance & Late Submission Policy: Assignments submitted after deadline up to 24 hours will have 20% deducted; between 24 hours and 48 will have an additional 20% deducted. Any submission later than 48 hours will not be accepted.

Academic Integrity:
Cheating and Plagiarism will not be tolerated. Professional integrity is an important aspect of all engineering disciplines, and understanding the material in these courses is integral to becoming a proficient and productive engineer. As such, it is imperative that you spend the time and effort to fully understand the material. Please read the UC Davis "Code of Academic Conduct" for further details: http://sja.ucdavis.edu/cac.html

Course Content and approximate timeline:

Week	Date	Lecture	Topic	Lab
½	-	-	-	-
	9/24	1	Intro to cleanroom, rules & safety training	
1	9/29	2	MOSFET layout, cross-section, intro to process flow	**1** Safety, gowning, piranha clean
	10/1	3	Photolithography, pattern transfer	
2	10/6	4	Oxidation	**2** 1st mask, oxide etching
	10/8	-	**NO CLASS**	
3	10/13	5	Oxidation & wet chemical etch	**3** Characterization (Morphology)
	10/15	6	Diffusion	
4	10/20	7	Diffusion (cont.)	**4** 2nd mask, gate removal
	10/22	8	Sheet resistance, junction depth	
5	10/27	9	Dry etching, (an)isotropic etching	**5** Characterization (Electrical)
	10/29	-	**MIDTERM**	
6	11/3	10	Ion implantation, annealing	**6** 3rd mask, gate & contact etch
	11/5	11	Ion implantation, annealing (cont.)	
7	11/10	12	Physical vapor deposition (PVD)	**NO LAB**
	11/12	13	Chemical vapor deposition (CVD)	
8	11/17	14	Metal-semiconductor interface	**7** 4th mask, interconnects
	11/19	15	Characterization techniques	
9	11/24	16	Process monitoring, dicing, wire bonding, packaging	**NO LAB**
	11/26	-	**THANKSGIVING**	
10	12/1	17	Biological microsystems & nanotechnology	**8** Characterization (Device)
	12/3	-	**REVIEW**	